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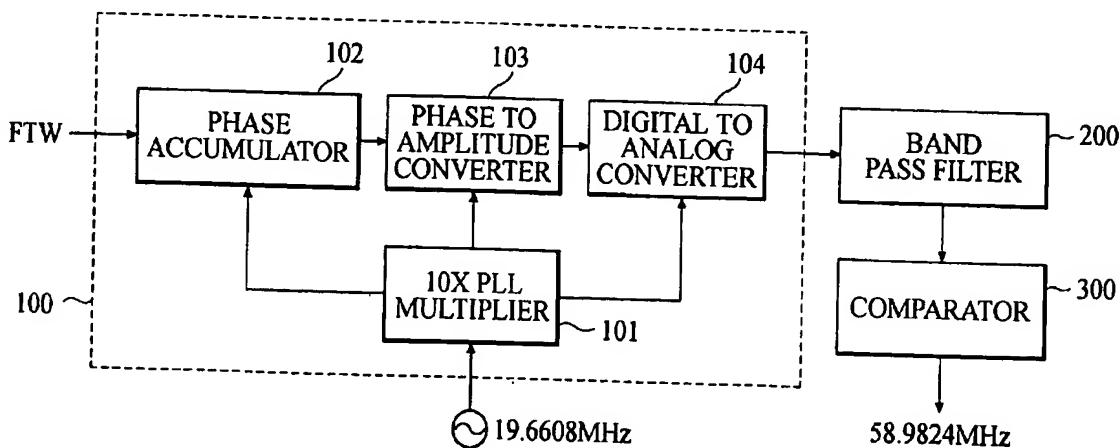
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(54) Title: APPARATUS FOR GENERATING CLOCK PULSES USING A DIRECT DIGITAL SYNTHESIZER



(57) Abstract: The present invention relates to an apparatus for generating clock pulses using a Direct Digital Synthesizer (DDS). The present invention seeks to solve the problems of the conventional clock generator using a Phase Locked Loop (PLL) circuit where the output clock frequency cannot be varied and the output clock signal is degraded because of jitter and phase noise. The claimed apparatus comprises a phase accumulator, a phase-to-magnitude converter, a Digital-to-Analog (DA) converter, a band pass filter, and a comparator, which are serially connected. A 10XPLL multiplier provides a 196.608MHz clock signal to the phase accumulator, the phase-magnitude converter and the digital analog converter, respectively. The phase accumulator also receives a Frequency Tuning Word (FTW) and using this FTW and the 196.608MHz clock, outputs a desired specific frequency value. This in order to become a square wave of a desired frequency with a low jitter.